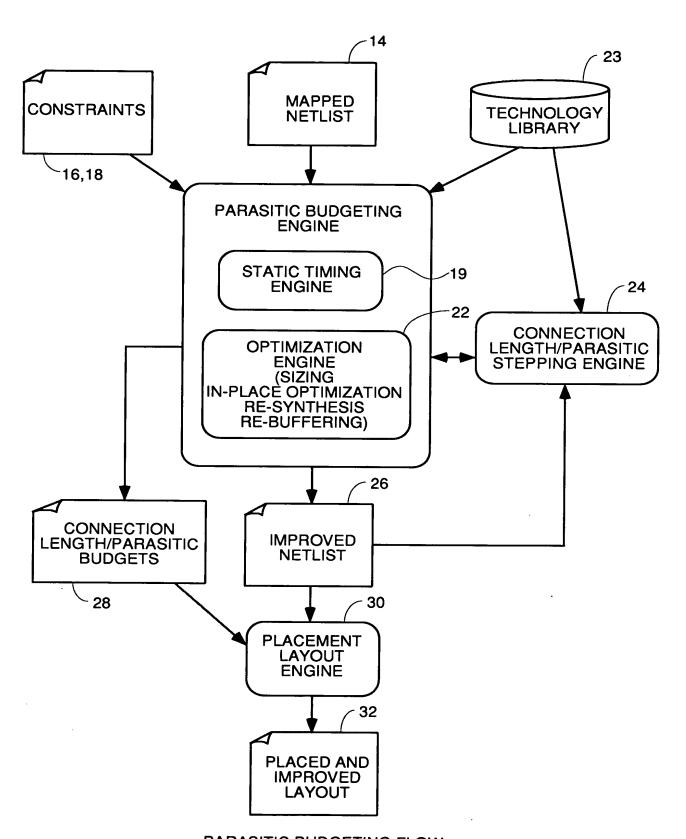
Application No.: 10/774,853 Inventor: CHEN, et al. Docket No.: SIL-001 OIPE METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC **BUDGETING** JUL 2 7 2004 1/17 -10 LANGUAGE OR **NETLIST** 21 **CONSTRAINTS** SYNTHESIS COMPONENT -16 OR LIBRARY MAPPING **POWER** -23 14 CONSTRAINTS (ACTIVITY) TECHNOLOGY **MAPPED** INFORMATION **NETLIST** 20 CONNECTION **PARASITIC** LENGTH/PARASITIC BUDGETING STEPPING **ENGINE ENGINE** -28 26 CONNECTION **IMPROVED** LENGTH/PARASITIC **NETLIST BUDGETS** 30 **PLACEMENT LAYOUT ENGINE √32 PLACED AND IMPROVED LAYOUT**

PARASITIC BUDGETING FLOW

FIG. 1

BUDGETING

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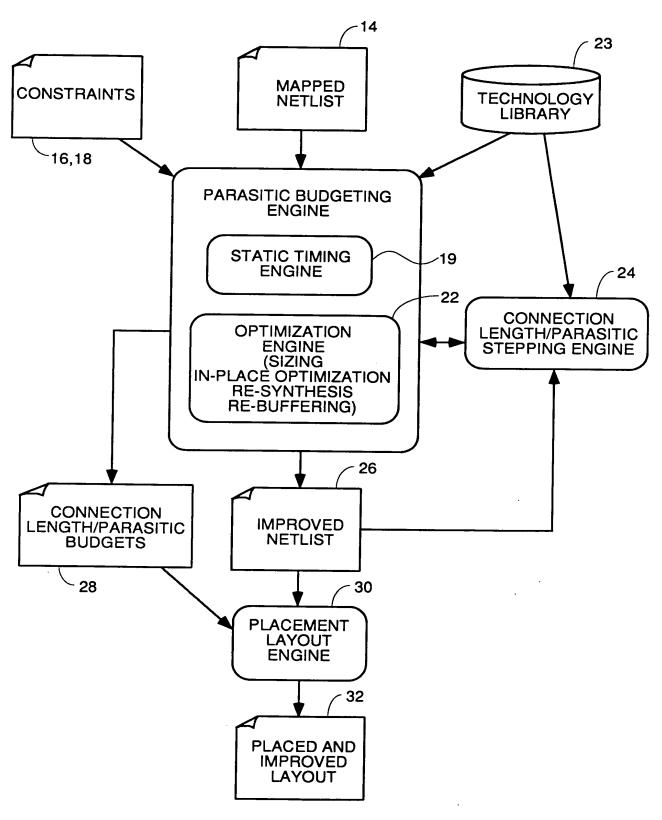


PARASITIC BUDGETING FLOW

FIG. 2A

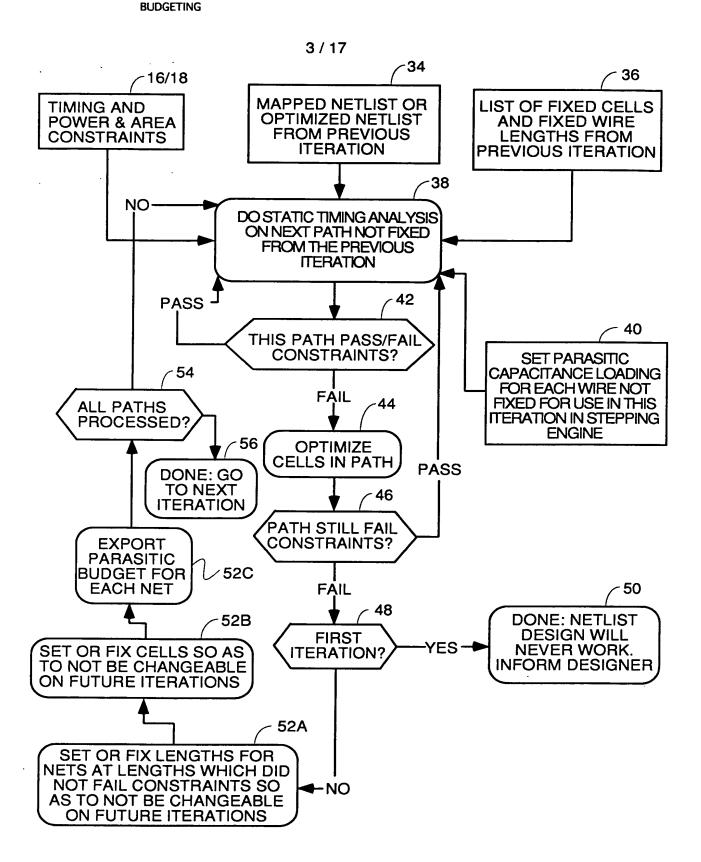
Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC BUDGETING

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PARASITIC BUDGETING FLOW

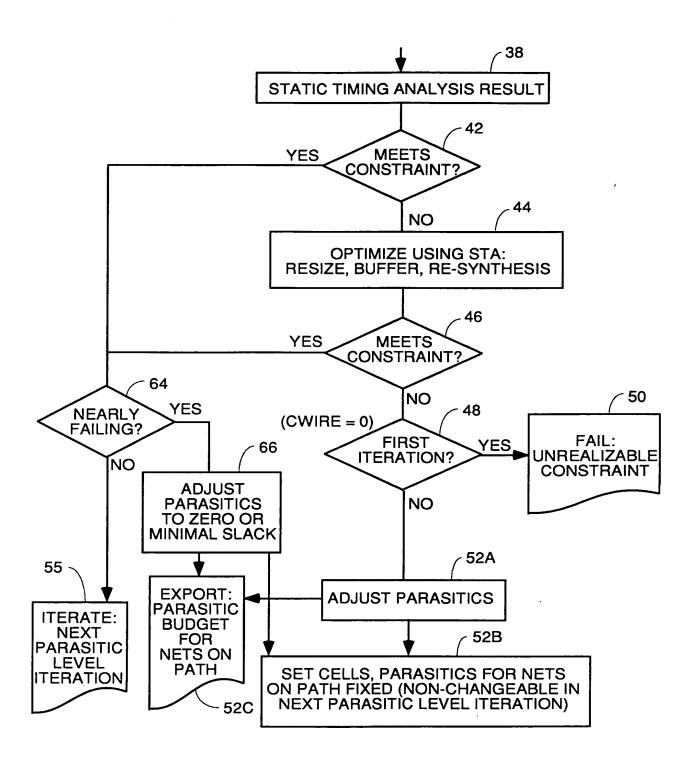
FIG. 2A



PROCESS FLOW FOR ONE ITERATION OF THE ITERATIVE PARASITIC BUDGET OPTIMIZATION PROCESS

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC BUDGETING

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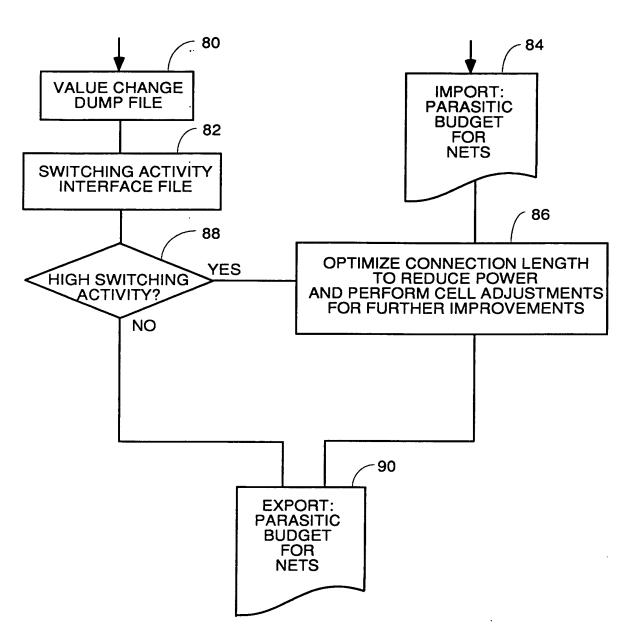


ALTERNATE IMPLEMENTATION FLOW FOR EACH PATH INSIDE EACH PARASITIC LEVEL ITERATION.

FIG. 2C

BUDGETING

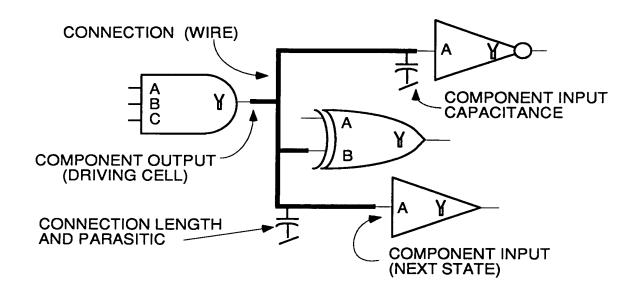




ALTERNATE IMPLEMENTATION FLOW POWER OPTIMIZATION OF PARASITIC BUDGET

BUDGETING

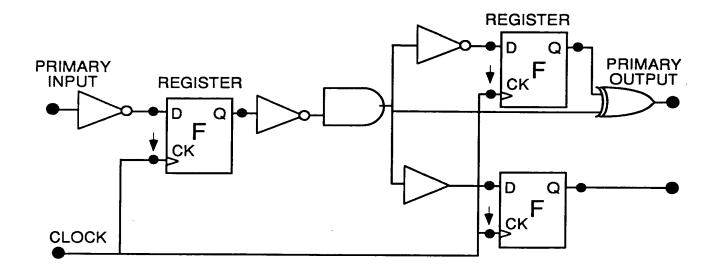
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CRITICAL PATH STAGE ELEMENT

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC BUDGETING

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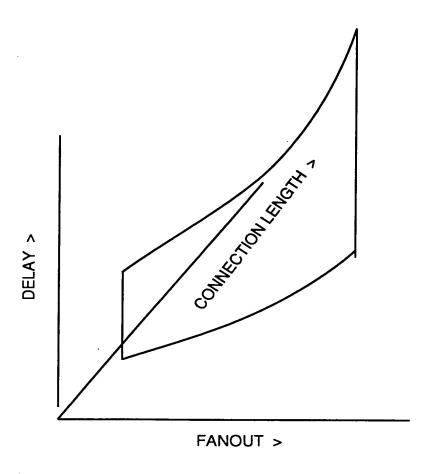


CRITICAL PATH REGISTER STRUCTURE

FIG. 4

BUDGETING

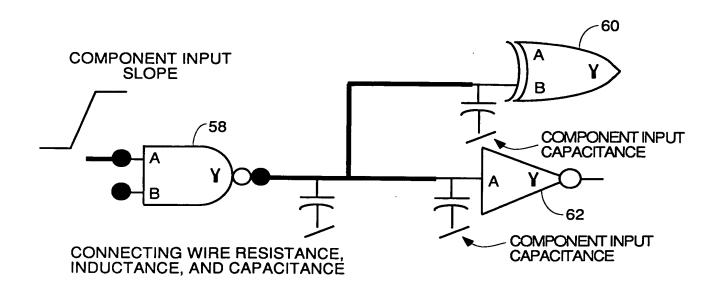
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DELAY AS FUNCTION OF FANOUT AND CONNECTION LENGTH

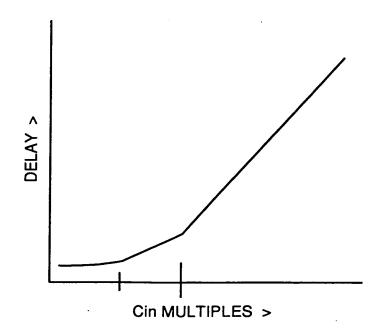
BUDGETING

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PARASITIC ELEMENTS CONTRIBUTING TO CELL DELAY (NAND2 WITH FANOUT=2)

FIG. 6A



DELAY OF A NAND2 COMPONENT AS A FUNCTION OF Cin MULTIPLIES

FIG. 6B

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC

BUDGETING

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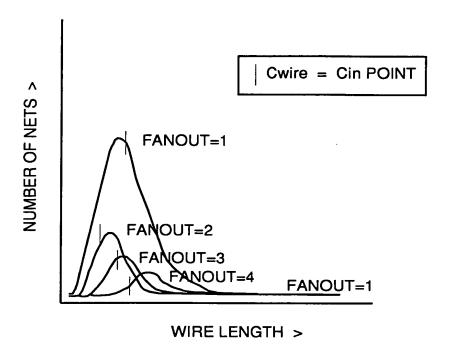
TECHNOLOGY NODE	Cin (pf)	LENGTH (um)			
	AVERAGE	Cwire=Cin			
CMOS 90nm	0.0025	6.02			
CMOS 0.13um	0.0052	23.99			
CMOS 0.18um	0.0079	40.63			
CMOS 0.25um	0.0154	104.84			

CONNECTION LENGTH WHERE Cwire MATCHES Cin AS FUNCTION OF PROCESS

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC

BUDGETING

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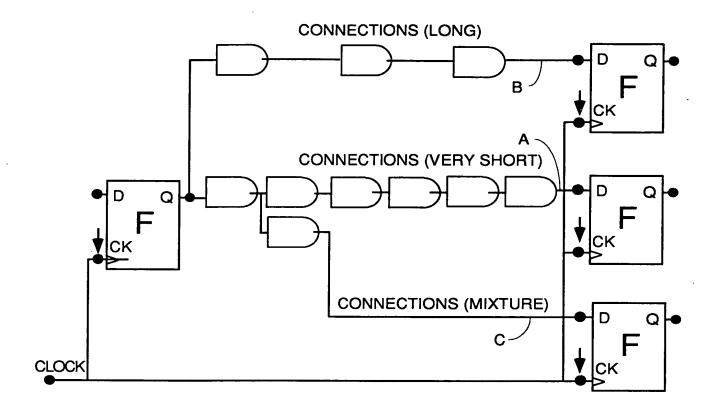


DISTRIBUTION OF CONNECTION LENGTHS BY FANOUT IN A TYPICAL CIRCUIT

FIG. 8

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC BUDGETING

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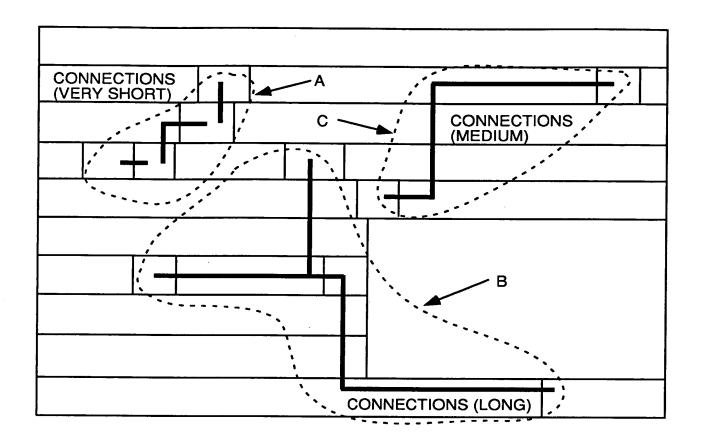
SYMBOLIC REPRESENTATION OF CRITICAL PATHS THAT CAN HAVE DIFFERENT CONNECTION LENGTHS AND MEET TIMING

FIG. 9

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC

BUDGETING

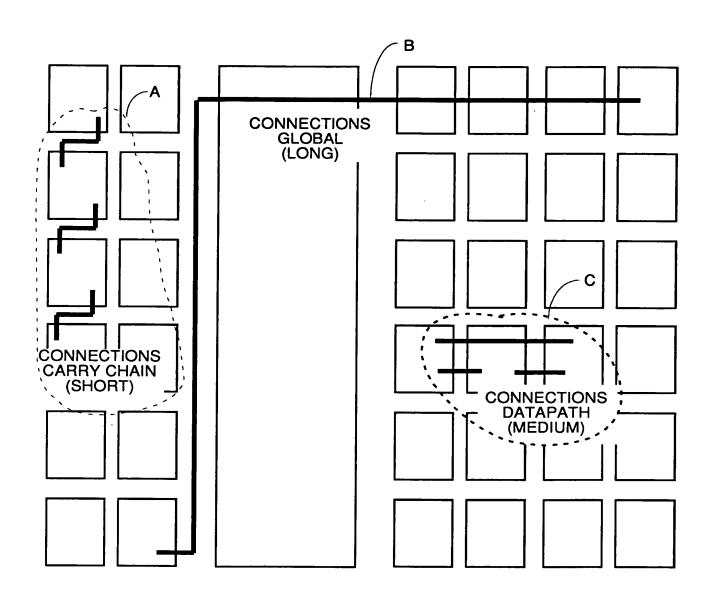
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TYPICAL STANDARD CELL ROW LAYOUT WITH SHORT AND LONG CONNECTIONS

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC BUDGETING

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TYPICAL FIELD PROGRAMMABLE GATE ARRAY CONNECTIONS WITH SPECIAL SHORT AND LONG CONNECTIONS

FIG. 11

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC

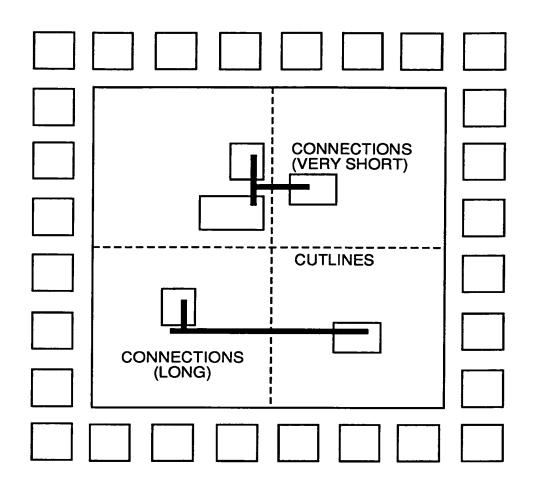
BUDGETING

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_ _		8	8	72	4	22	9	16	ھ	4	2	1
PHYSICAL	WEIGHT											
HIERARCHY	CLASS	0.1 SIMPLE	0.4 SIMPLE	SIMPLE	1.7 SIMPLE	4.0 SIMPLE	4.0 COMPLEX	10.6 SIMPLE	33.4 SIMPLE	57.1 SIMPLE	57.1 COMPLEX	
Cin	MULTIPLE	0.1	0.4	1.0	1.7	4.0	4.0	10.6	33.4	57.1	57.1	
PARASITIC	(SIMPLE CAP)	0.0007	0.0021	0.0050	0.0086	0.0200	0.0200	0.0529	0.1668	0.2857	0.2857	
CONNECTION LENGTH	(NM)	2.00	00.9	14.00	24.00	26.00	26.00	148.00	467.00	800.00	800.00	

CONNECTION LENGTH FROM A PARASITIC BUDGET TRANSLATION TO WEIGHTS FOR PLACEMENT AND PARTITIONING

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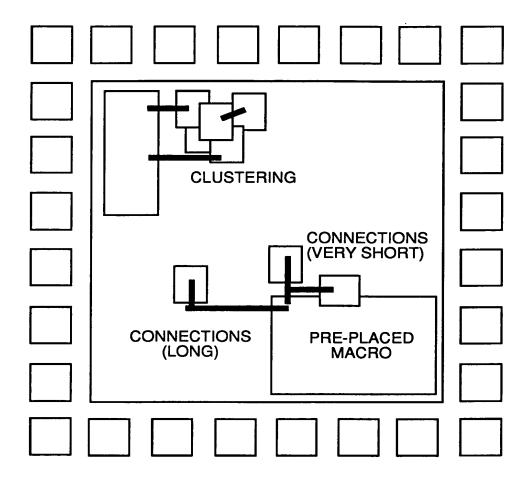
CONNECTION LENGTH CLUSTERING AROUND A PLACEMENT OR PARTITIONING CUTLINE

FIG. 13

Title: METHOD OF OPTIMIZING IC LOGIC PERFORMANCE BY STATIC TIMING BASED PARASITIC

BUDGETING

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PLACEMENT CLUSTERING BASED ON CONNECTION LENGTH FROM A PARASITIC BUDGET

FIG. 14